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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	09/559,903
	Filing Date	April 26, 2000
	First Named Inventor	Zhiping Yin
	Art Unit	2815
	Examiner Name	G. Eckert II
Total Number of Pages in This Submission	Attorney Docket Number	MI22-1427

ENCLOSURES (Check all that apply)		
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Firm or Individual	Jennifer J. Taylor, Ph.D.; Reg. No. 48,711; Wells St. John P.S.
Signature	<i>Jennifer J. Taylor</i>
Date	December 18, 2003

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EL979950463



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/559,903  
Filing Date .... April 26, 2000  
Inventor .... Zhiping Yin et al.  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 2815  
Examiner .... G. Eckert II  
Attorney's Docket No. .... MI22-1427  
Title: Circuitry and Gate Stacks

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449.

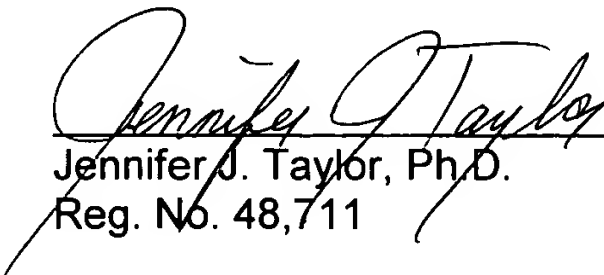
No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.


Citation of these references is respectfully requested.

Respectfully submitted,

Date: 12-18-2003

  
Jennifer J. Taylor, Ph.D.  
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1427		SERIAL NO. 09/559,903	
 LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Zhiping Yin et al.			
				FILING DATE April 26, 2000		GROUP 2815	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,133,618	10-2000	Steiner			
	AB	5,994,217	11-1999	Ng			
	AC	5,985,519	11-1999	Kakamu et al.			
	AD	5,747,388	05-1998	Küstters et al.			
	AE	5,639,687	06-1997	Roman et al.			
	AF	5,498,555	03-1996	Lin			
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AM						
	AN						
	AO						
	AP						
	AQ						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	A		Wolf, S., "Silicon Processing for the VLSI Era," Vol. 1, pps. 407-413.				
	R						
	AS		Wolf, S. "Silicon Processing for the VLSI Era", Vol. 2, pgs. 48-49 and 435.				
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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